Low Voltage, High Frequency Four-Quadrant CMOS Current Multiplier Circuit

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Abstract

This paper proposes a high frequency four-quadrant CMOS current multiplier circuit using low voltage supply. This circuit has frequency response about 15 GHz, using $\pm 1V$ supply voltage and has input range about $\pm 15\mu A$. All CMOSs operate in saturation region and the simulation results are based on 0.18 μm CMOS technology achieved using HSPICE (Level 49).

1. Introduction

Current multiplier circuit is a basic circuit to apply to make other circuit. Some application use current multiplier, for example modulator. This paper proposes frequency four-quadrant CMOS current multiplier circuit based on 0.18 μm *CMOS* technology.

2. Circuit Description

Let's

$$A = (a+b+c)^2,\ B = (-a-b+c)^2$$
$$C = (a-b+d)^2,\ D = (-a+b+d)^2$$

So

$$(A+B)-(C+D) = 8ab$$

The proposed current multiplier circuit consist of current copier and apply to current adder and current sub tractor, I to V converter, Inverter, V to I converter with current copier to get output signal inform of multiply. All CMOSs operate in saturation region.

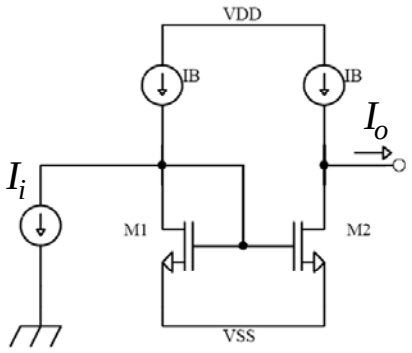

Figure 1. Current Copier

Figure 1 is a current copier circuit that the direction of input and output is opposite. If the circuit sinks I_{in} at the input, then it will source I_{in} at the output. If the circuit sources I_{in} at the input, then circuit will sink I_{in} at the output.

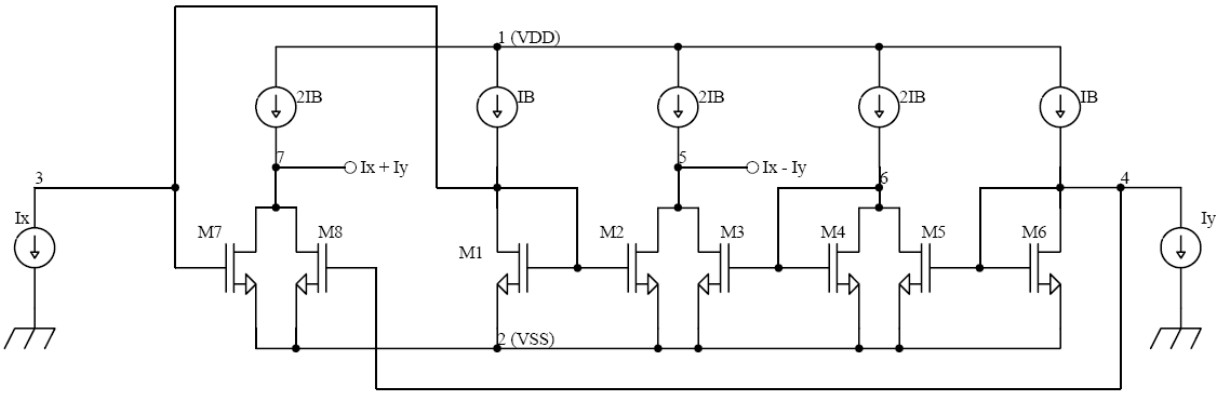

Figure 2. Current adder $I_X + I_Y$ and current sub tractor

$$V_{GS1} = V_{GS2} \quad (1)$$

So $$I_{D1} = I_{D2} \quad (2)$$

$$I_B - I_i = I_B - I_o \quad (3)$$

Since the direction of the currents are opposite, then

$$I_o = -I_i \quad (4)$$

Mixing the current copiers such like Figure 2, we get a current adder $I_X + I_Y$ and current sub tractor $I_X - I_Y$.

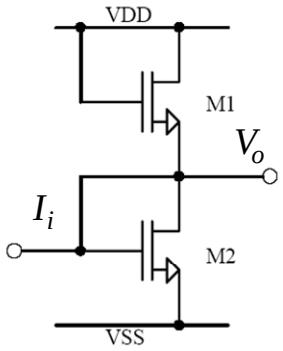

Figure 3. I to V Converter

Figure 3 is an I to V converter that consists of 2 same aspect ratio of MOSs and operates in the saturation region.

When $K_n = \mu_n C_{ox} \frac{W}{L} = K_1$ (5)

$$I_{D1} = \frac{K_1}{2}(V_{DD} - V_o - V_T)^2 \quad (6)$$

$$I_{D2} = \frac{K_1}{2}(V_0 - V_{SS} - V_T)^2 \quad (7)$$

$$V_{DD} - V_T = -(V_{SS} + V_T) \quad (8)$$

$$I_{in} = I_{D2} - I_{D1} \quad (9)$$

$$I_{in} = 2K_1 V_o (V_{DD} - V_T) \quad (10)$$

$$V_o = \frac{I_i}{2K_1(V_{DD} - V_T)} \quad (11)$$

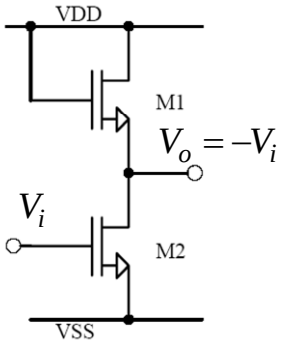

Figure 4. Inverter

Figure 4 is an inverter that consists of 2 same aspect ratio of MOSs and operates in saturation region.

$$I_{D1} = \frac{K_1}{2}\left(V_{DD} - V_o - V_T\right)^2 \quad (12)$$

$$I_{D2} = \frac{K_1}{2}\left(V_i - V_{SS} - V_T\right)^2 \quad (13)$$

$$V_{GS1} = V_{GS2} \quad (14)$$

$$V_{DD} - V_o = V_i - V_{SS} \quad (15)$$

$$V_o = -V_i \quad (16)$$

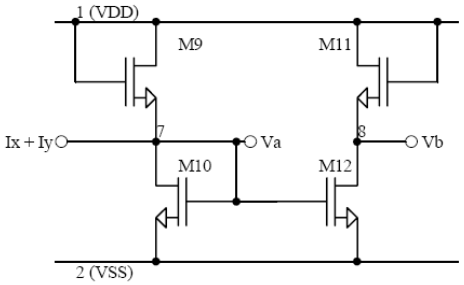

Figure 5. I to V converter and Inverter with feed input of $I_X + I_Y$

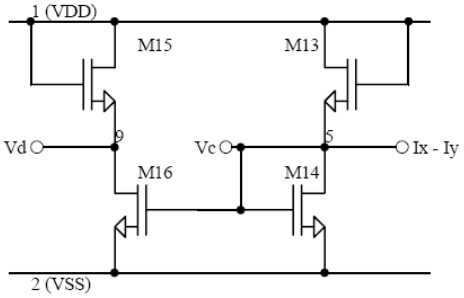

Figure 6. I to V converter and Inverter with feed input of $I_X - I_Y$

Merging the I to V converter and the inverter, as shown in Figure 5 and Figure 6, yields the nodes V_A, V_B, V_C and V_D voltages bellow

$$V_A = \frac{I_X + I_Y}{2K_1\left(V_{DD} - V_T\right)} \quad (17)$$

$$V_B = \frac{-I_X - I_Y}{2K_1\left(V_{DD} - V_T\right)} \quad (18)$$

$$V_C = \frac{I_X - I_Y}{2K_1\left(V_{DD} - V_T\right)} \quad (19)$$

$$V_D = \frac{-I_X + I_Y}{2K_1\left(V_{DD} - V_T\right)} \quad (20)$$

V_A, V_B, V_C and V_D feed to M_{17}, M_{18}, M_{19} and M_{20}, as shown in Figure 7, all of 4 MOSs have same aspect ratio MOSs and operate in saturation region

Let

$$K_n = \mu_n C_{ox}\frac{W}{L} = K_2 \quad (21)$$

$$a = 2K_1\left(V_{DD} - V_T\right) \quad (22)$$

$$b = -\left(V_{SS} + V_T\right) \quad (23)$$

The Drain currents of each MOS are

$$I_{D17} = \frac{K_2}{2}\left(\frac{I_X}{a} + \frac{I_Y}{a} + b\right)^2 \quad (24)$$

$$I_{D18} = \frac{K_2}{2}\left(-\frac{I_X}{a} - \frac{I_Y}{a} + b\right)^2 \quad (25)$$

$$I_{D19} = \frac{K_2}{2}\left(\frac{I_X}{a} - \frac{I_Y}{a} + b\right)^2 \quad (26)$$

$$I_{D20} = \frac{K_2}{2}\left(-\frac{I_X}{a} + \frac{I_Y}{a} + b\right)^2 \quad (27)$$

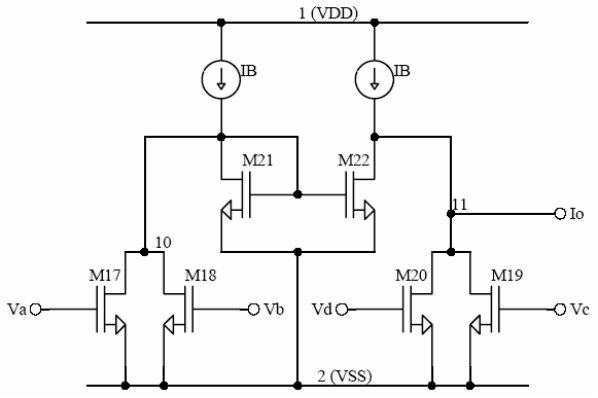

Figure 7. V to I converter with current copier

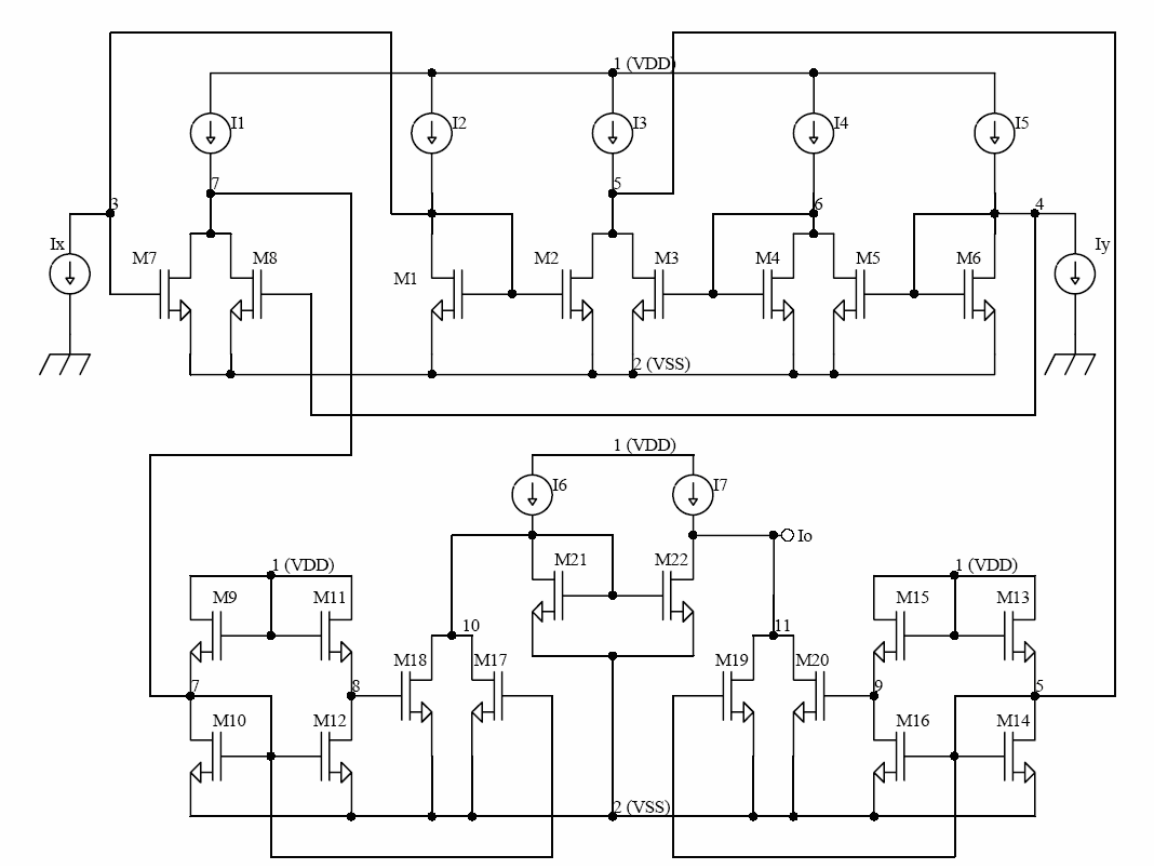

Figure 8. Current multiplier

M_{21} and M_{22} in Figure7 are current copier and act to subtract the current of $(I_{D17} + I_{D18}) - (I_{D19} + I_{D2o})$

$$I_{D17} + I_{D18} = \frac{K_2}{2}\left(\frac{2I_X^2}{a^2} + \frac{2I_Y^2}{a^2} + 2b^2 + \frac{4I_X I_Y}{a^2}\right) \quad (28)$$

$$I_{D19} + I_{D20} = \frac{K_2}{2}\left(\frac{2I_X^2}{a^2} + \frac{2I_Y^2}{a^2} + 2b^2 - \frac{4I_X I_Y}{a^2}\right) \quad (29)$$

$$I_o = (I_{D17} + I_{D18}) - (I_{D19} + I_{D2o}) \quad (30)$$

$$I_o = \frac{4K_2 I_X I_Y}{a^2} \quad (31)$$

$$I_o = \frac{K_2 I_X I_Y}{K_1^2 (V_{DD} - V_T)^2} \quad (32)$$

3. Results

The complete circuit of the current multiplier is viewed in Figure 8, and the simulation use 0.18µm CMOS and simulate with H-Spice level 49 MOS aspect ratio shown in Table 1. Current source is showing in Table 2.

The simulation result of the DC characteristic can be seen in Figure 9. Input of I_x and I_y current are -15µA to +15µA by I_x increase from -15µA to +15µA and I_y sweep from -15µA to +15µA in 7 (seven) steps, as we can see in Figure 9.

Table 1. Aspect ratio of MOS transistor

MOS transistor	W/L
M1-M16, M21-M22	0.3/0.3
M17-M20	0.3/0.6

Table 2. Current Source

Current Source	Current
I1, I3, I4	$30\mu A$
I2, I5	$15\mu A$
I6, I7	$40\mu A$

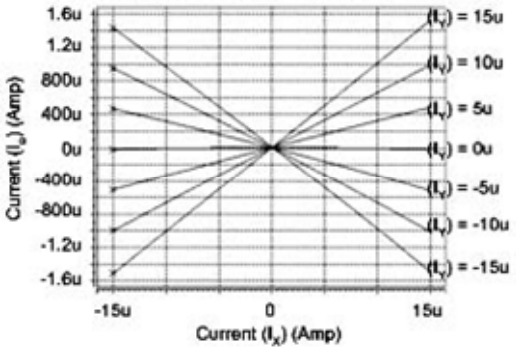

Figure 9. DC Characteristics

Figure 10 shows about frequency response. The frequency increases from 100 kHz to 100 GHz. The simulation result measures that -3dB of the frequency is about 15 GHz.

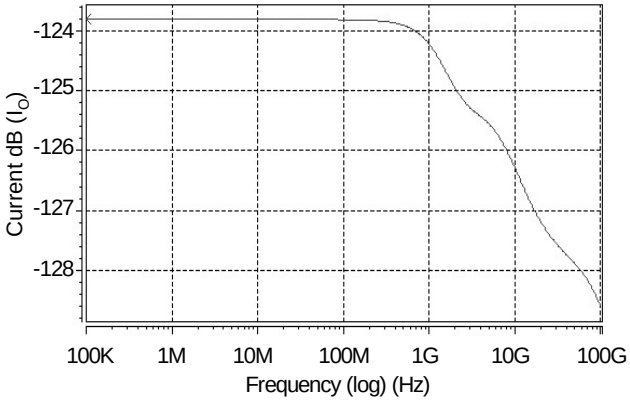

Figure 10 Frequency Response

Figure 11 shows about the total harmonic distortion (THD). We feed I_y current 2 values that are -10μA and +10 μA. I_x is sine wave by amplitude 10μA, and the frequency from 10 kHz to 10 GHz.

The period of consider frequency is

$$T_{STOP} = \frac{2}{f} \qquad (33)$$

And the step is

$$T_{STEP} = \frac{2}{100\,f} \qquad (34)$$

As seen in the THD graph, when I_y is -10μA,that THD is approximately 1.4% until the frequency increase to 10 MHz, where THD starts to increase. The graph shows that the maximum THD is 7.5% at 1 GHz. When I_y is +10μA, THD is approximately 1.2% until the frequency increase to 10 MHz, where THD starts to increase. The maximum THD is 5.4% at 9 GHz.

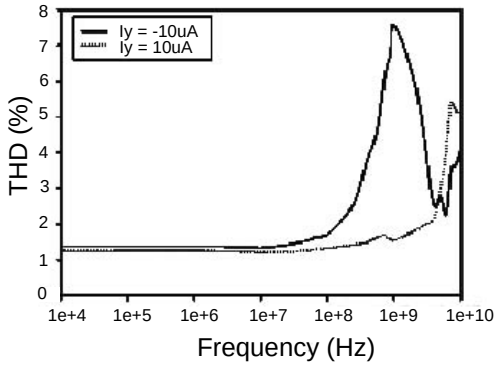

Figure 11 Total harmonic distortions

The next is about the multiplier circuit that is applied in modulator. I_x is

$10\mu A_{P-P}$ and has frequency 500 MHz, while I_y is a carrier signal, with frequency 5 GHz, and amplitude $5\mu A_{P-P}$ as we can see in Figure 12 and Figure 13. The modulated frequency is shown in Figure 14.

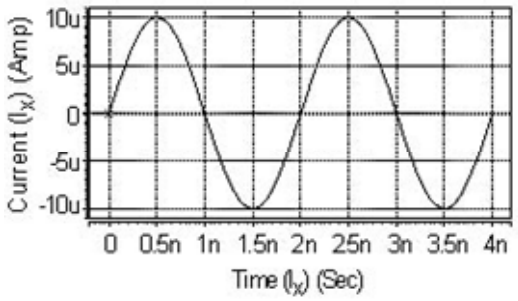

Figure 12 Signal, frequency 500 MHz and amplitude $10\mu A_{P-P}$

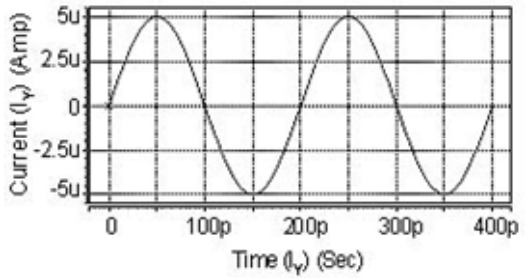

Figure 13 Carrier signal, frequency 5 GHz, and amplitude $5\mu A_{P-P}$

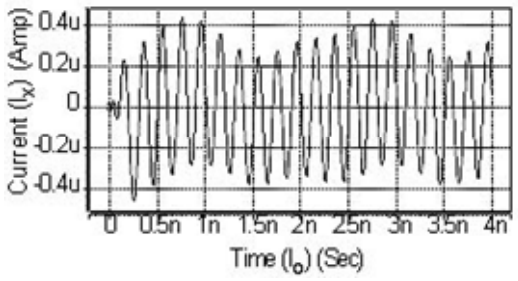

Figure 14 Modulated output Signal

4. Conclusion

A current multiplier circuit using $\pm 1V$ voltage supply is proposed in this article. Frequency response of the circuit is 15 GHz. Other Value of Simulation is shown in Table 3.

Table 3 Other Value of Simulation and simulation result

Parameter	Value
Technology	0.18 μm *CMOS*
Supply Voltage	$\pm 1V$
CMOS amount	22
Current Source amount	7
Input Range	$\pm 15\mu A$
Bandwidth (-3 dB)	15 GHz
Power dissipation	0. 681m watts

5. References

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