Low Voltage, High Frequency Four-Quadrant CMOS Current Multiplier Circuit

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Abstract
This paper proposes a high frequency four-quadrant CMOS current multiplier circuit using low voltage supply. This circuit has frequency response about 15 GHz, using ±1V supply voltage and has input range about ±15μA. All CMOSs operate in saturation region and the simulation results are based on 0.18 μm CMOS technology achieved using HSPICE (Level 49).

1. Introduction
Current multiplier circuit is a basic circuit to apply to make other circuit. Some application use current multiplier, for example modulator. This paper proposes frequency four-quadrant CMOS current multiplier circuit based on 0.18 μm CMOS technology.

2. Circuit Description
Let’s
\[
A = (a + b + c)^2, \quad B = (-a - b + c)^2
\]
\[
C = (a - b + d)^2, \quad D = (-a + b + d)^2
\]
So
\[
(A + B) - (C + D) = 8ab
\]

Figure 1 is a current copier circuit that the direction of input and output is opposite. If the circuit sinks \( I_{in} \) at the input, then it will source \( I_{in} \) at the output. If the circuit sources \( I_{in} \) at the input, then circuit will sink \( I_{in} \) at the output.
Since the direction of the currents are opposite, then

\[ I_o = -I_i \]  \hspace{2cm} (4)

Mixing the current copiers such like Figure 2, we get a current adder \( I_x + I_y \) and current sub tractor \( I_x - I_y \).
\[ I_{D1} = \frac{K_1}{2} (V_{DD} - V_o - V_T) \] (12)

\[ I_{D2} = \frac{K_1}{2} (V_i - V_{SS} - V_T) \] (13)

\[ V_{GS1} = V_{GS2} \] (14)

\[ V_{DD} - V_o = V_i - V_{SS} \] (15)

\[ V_o = -V_i \] (16)

\[ V_D = \frac{-I_X + I_Y}{2K_1(V_{DD} - V_T)} \] (20)

\[ V_A, V_B, V_C \] and \[ V_D \] feed to \[ M_{17}, M_{18}, M_{19} \] and \[ M_{20} \], as shown in Figure 7, all of 4 MOSs have same aspect ratio MOSs and operate in saturation region.

Let

\[ K_n = \mu_n C_{ox} \frac{W}{L} = K_2 \] (21)

\[ a = 2K_1(V_{DD} - V_T) \] (22)

\[ b = -(V_{SS} + V_T) \] (23)

The Drain currents of each MOS are

\[ I_{D17} = \frac{K_2}{2} \left( \frac{I_X + I_Y}{a} + b \right)^2 \] (24)

\[ I_{D18} = \frac{K_2}{2} \left( \frac{-I_X - I_Y}{a} + b \right)^2 \] (25)

\[ I_{D19} = \frac{K_2}{2} \left( \frac{I_X - I_Y}{a} + b \right)^2 \] (26)

\[ I_{D20} = \frac{K_2}{2} \left( \frac{-I_X + I_Y}{a} + b \right)^2 \] (27)

Figure 7. V to I converter with current copier
$M_{21}$ and $M_{22}$ in Figure 7 are current copier and act to subtract the current of $(I_{D17} + I_{D18}) - (I_{D19} + I_{D20})$

$$I_{D17} + I_{D18} = \frac{K_x}{2} \left( \frac{2I_x^2}{a^2} + \frac{2I_y^2}{a^2} + 2b^2 + \frac{4I_x I_y}{a^2} \right)$$  \hspace{1cm} (28)$$

$$I_{D19} + I_{D20} = \frac{K_x}{2} \left( \frac{2I_x^2}{a^2} + \frac{2I_y^2}{a^2} + 2b^2 - \frac{4I_x I_y}{a^2} \right)$$  \hspace{1cm} (29)$$

$$I_o = (I_{D17} + I_{D18}) - (I_{D19} + I_{D20})$$  \hspace{1cm} (30)$$

$$I_o = \frac{4K_x I_x I_y}{a^2}$$  \hspace{1cm} (31)$$

$$I_o = \frac{K_x I_x I_y}{K_1 (V_{DD} - V_T)}$$  \hspace{1cm} (32)$$

3. Results

The complete circuit of the current multiplier is viewed in Figure 8, and the simulation use 0.18µm CMOS and simulate with H-Spice level 49 MOS aspect ratio shown in Table 1. Current source is showing in Table 2.

The simulation result of the DC characteristic can be seen in Figure 9. Input of $I_x$ and $I_y$ current are -15µA to +15µA by $I_x$ increase from -15µA to +15µA and $I_y$ sweep from -15µA to +15µA in 7 (seven) steps, as we can see in Figure 9.
Table 1. Aspect ratio of MOS transistor

<table>
<thead>
<tr>
<th>MOS transistor</th>
<th>W/L</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-M16, M21-M22</td>
<td>0.3/0.3</td>
</tr>
<tr>
<td>M17-M20</td>
<td>0.3/0.6</td>
</tr>
</tbody>
</table>

Table 2. Current Source

<table>
<thead>
<tr>
<th>Current Source</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>I1, I3, I4</td>
<td>30µA</td>
</tr>
<tr>
<td>I2, I5</td>
<td>15µA</td>
</tr>
<tr>
<td>I6, I7</td>
<td>40µA</td>
</tr>
</tbody>
</table>

Figure 9. DC Characteristics

Figure 10 shows about frequency response. The frequency increases from 100 kHz to 100 GHz. The simulation result measures that -3dB of the frequency is about 15 GHz.

Figure 10 Frequency Response

Figure 11 shows about the total harmonic distortion (THD). We feed $I_y$ current 2 values that are -10µA and +10 µA. $I_x$ is sine wave by amplitude 10µA, and the frequency from 10 kHz to 10 GHz.

The period of consider frequency is

$$T_{STOP} = \frac{2}{f} \quad (33)$$

And the step is

$$T_{STEP} = \frac{2}{100f} \quad (34)$$

As seen in the THD graph, when $I_y$ is -10µA, that THD is approximately 1.4% until the frequency increase to 10 MHz, where THD starts to increase. The graph shows that the maximum THD is 7.5% at 1 GHz. When $I_y$ is +10µA, THD is approximately 1.2% until the frequency increase to 10 MHz, where THD starts to increase. The maximum THD is 5.4% at 9 GHz.

Figure 11 Total harmonic distortions

The next is about the multiplier circuit that is applied in modulator. $I_x$ is
10μA_{p-p} and has frequency 500 MHz, while \( I_y \) is a carrier signal, with frequency 5 GHz, and amplitude 5μA_{p-p}, as we can see in Figure 12 and Figure 13. The modulated frequency is shown in Figure 14.

4. Conclusion

A current multiplier circuit using ±1V voltage supply is proposed in this article. Frequency response of the circuit is 15 GHz. Other Value of Simulation is shown in Table 3.

Table 3 Other Value of Simulation and simulation result

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18 μm CMOS</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>±1V</td>
</tr>
<tr>
<td>CMOS amount</td>
<td>22</td>
</tr>
<tr>
<td>Current Source amount</td>
<td>7</td>
</tr>
<tr>
<td>Input Range</td>
<td>±15μA</td>
</tr>
<tr>
<td>Bandwidth (-3 dB)</td>
<td>15 GHz</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>0.681 m watts</td>
</tr>
</tbody>
</table>

5. References


