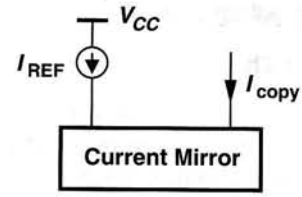

Figure 9.22 Concept of current mirror.

The bandgap circuit by itself does not solve all of our problems! An integrated circuit may incorporate hundreds of current sources, e.g., as the load impedance of CE or CS stages to achieve a high gain. Unfortunately, the complexity of the bandgap prohibits its use for each current source in a large integrated circuit.

Let us summarize our thoughts thus far. In order to avoid supply and temperature dependence, a bandgap reference can provide a "golden current" while requiring a few tens of devices. We must therefore seek a method of "copying" the golden current without duplicating the entire bandgap circuitry. Current mirrors serve this purpose.

Figure 9.22 conceptually illustrates our goal here. The golden current generated by a bandgap reference is "read" by the current mirror and a copy having the same characteristics as those of I_{REF} is produced. For example, $I_{copy} = I_{REF}$ or $2I_{REF}$.

9.2.2 Bipolar Current Mirror

Since the current source generating I_{copy} in Fig. 9.22 must be implemented as a bipolar or MOS transistor, we surmise that the current mirror resembles the topology shown in Fig. 9.23(a), where Q_1 operates in the forward active region and the black box guarantees $I_{copy} = I_{REF}$ regardless of temperature or transistor characteristics. (The MOS counterpart is similar.)

How should the black box of Fig. 9.23(a) be realized? The black box generates an output voltage, $V_X(=V_{BE})$, such that Q_1 carries a current equal to I_{REF}:

$$I_{S1} \exp \frac{V_X}{V_T} = I_{REF}, \tag{9.86}$$

where the Early effect is neglected. Thus, the black box satisfies the following relationship:

$$V_X = V_T \ln \frac{I_{REF}}{I_{S1}}. \tag{9.87}$$

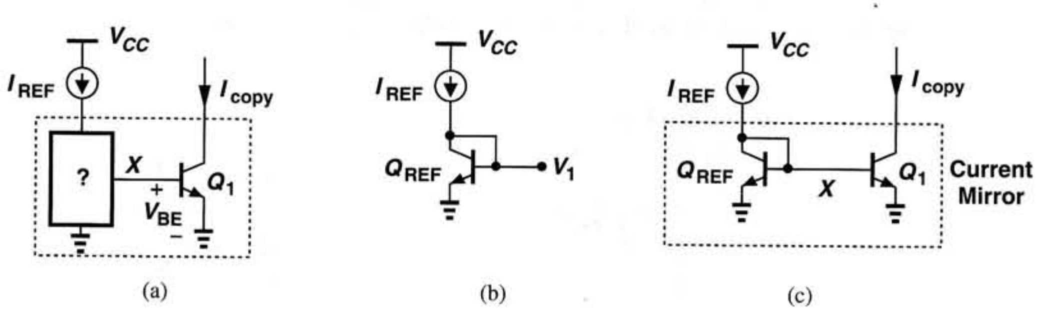

Figure 9.23 (a) Conceptual illustration of current copying, (b) voltage proportional to natural logarithm of current, (c) bipolar current mirror.

We must therefore seek a circuit whose output voltage is proportional to the natural logarithm of its input, i.e., the inverse function of bipolar transistor characteristics. Fortunately, a single diode-connected device satisfies (9.87). Neglecting the base-current in Fig. 9.23(b), we have

$$V_1 = V_T \ln \frac{I_{REF}}{I_{S,REF}}, \tag{9.88}$$

where $I_{S,REF}$ denotes the reverse saturation current of Q_{REF}. In other words, $V_1 = V_X$ if $I_{S,REF} = I_{S1}$, i.e., if Q_{REF} is identical to Q_1.

Figure 9.23(c) consolidates our thoughts, displaying the current mirror circuitry. We say Q_1 "mirrors" or copies the current flowing through Q_{REF}. For now, we neglect the base currents. From one perspective, Q_{REF} takes the natural logarithm of I_{REF} and Q_1 takes the exponential of V_X, thereby yielding $I_{copy} = I_{REF}$. From another perspective, since Q_{REF} and Q_1 have equal base-emitter voltages, we can write

$$I_{REF} = I_{S,REF} \exp \frac{V_X}{V_T} \tag{9.89}$$

$$I_{copy} = I_{S1} \exp \frac{V_X}{V_T} \tag{9.90}$$

and hence

$$I_{copy} = \frac{I_{S1}}{I_{S,REF}} I_{REF}, \tag{9.91}$$

which reduces to $I_{copy} = I_{REF}$ if Q_{REF} and Q_1 are identical. This holds even though V_T and I_S vary with temperature. Note that V_X does vary with temperature but in such a way that I_{copy} does not.

Example 9.12 An electrical engineering student who is excited by the concept of the current mirror constructs the circuit but forgets to tie the base of Q_{REF} to its collector (Fig. 9.24). Explain what happens.

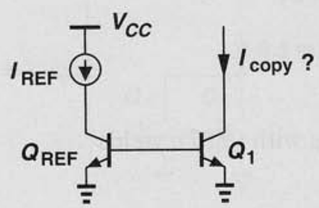

Figure 9.24

Solution The circuit provides no path for the base currents of the transistors. More fundamentally, the base-emitter voltage of the devices is not defined. The lack of the base currents translates to $I_{copy} = 0$.

Exercise What is the region of operation of Q_{REF}?

Example 9.13 Realizing the mistake in the above circuit, the student makes the modification shown in Fig. 9.25, hoping that the battery V_X provides the base currents and defines the base-emitter voltage of Q_{REF} and Q_1. Explain what happens.

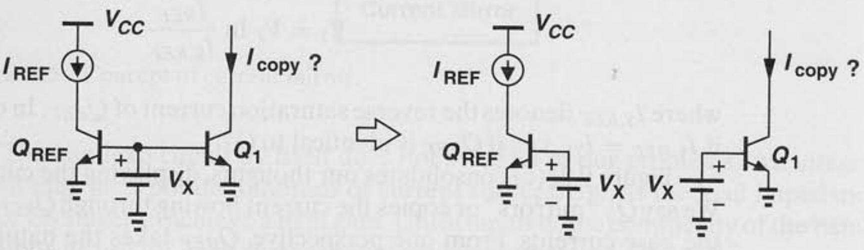

Figure 9.25

Solution While Q_1 now carries a finite current, the biasing of Q_1 is no different from that in Fig. 9.21; i.e.,

$$I_{copy} = I_{S1} \exp \frac{V_X}{V_T}, \tag{9.92}$$

which is a function of temperature if V_X is constant. The student has forgotten that a diode-connected device is necessary here to ensure that V_X remains proportional to $\ln(I_{REF}/I_{S,REF})$.

Exercise Suppose V_X is slightly greater than the necessary value, $V_T \ln(I_{REF}/I_{S,REF})$. In what region does Q_{REF} operate?

We must now address two important questions. First, how do we make additional copies of I_{REF} to feed different parts of an integrated circuit? Second, how do we obtain different values for these copies, e.g., $2I_{REF}$, $5I_{REF}$, etc.? Considering the topology in Fig. 9.22(c), we recognize that V_X can serve as the base-emitter voltage of multiple transistors, thus arriving at the circuit shown in Fig. 9.26(a). The circuit is often drawn as in Fig. 9.26(b) for simplicity. Here, transistor Q_j carries a current $I_{copy,j}$, given by

$$I_{copy,j} = I_{S,j} \exp \frac{V_X}{V_T}, \tag{9.93}$$

which, along with (9.87), yields

$$I_{copy,j} = \frac{I_{S,j}}{I_{S,REF}} I_{REF}. \tag{9.94}$$

The key point here is that multiple copies of I_{REF} can be generated with minimal additional complexity because I_{REF} and Q_{REF} themselves need not be duplicated.

Equation (9.94) readily answers the second question as well: If $I_{S,j}$ ($\propto$ the emitter area of Q_j) is chosen to be n times $I_{S,REF}$ ($\propto$ the emitter area of Q_{REF}), then $I_{copy,j} = nI_{REF}$. We say the copies are "scaled" with respect to I_{REF}. Recall from Chapter 4 that this is equivalent to placing n unit transistors in parallel. Figure 9.26(c) depicts an example where Q_1-Q_3 are identical to Q_{REF}, providing $I_{copy} = 3I_{REF}$.

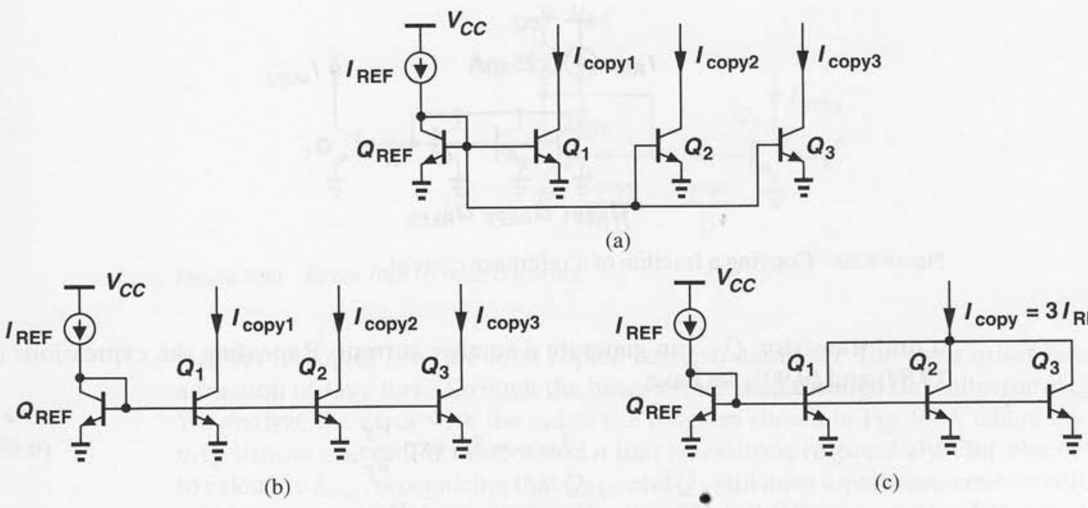

Figure 9.26 (a) Multiple copies of a reference current, (b) simplified drawing of (a), (c) combining output currents to generate larger copies.

Example 9.14 A multistage amplifier incorporates two current sources of values 0.75 mA and 0.5 mA. Using a bandgap reference current of 0.25 mA, design the required current sources. Neglect the effect of the base current for now.

Solution Figure 9.27 illustrates the circuit. Here, all transistors are identical to ensure proper scaling of I_{REF}.

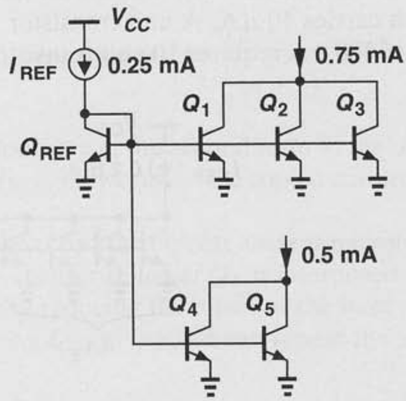

Figure 9.27

Exercise Repeat the above example if the bandgap reference current is 0.1 mA.

The use of multiple transistors in parallel provides an accurate means of scaling the reference in current mirrors. But, how do we create *fractions* of I_{REF}? This is accomplished by realizing Q_{REF} itself as multiple parallel transistors. Exemplified by the circuit in Fig. 9.28, the idea is to begin with a larger $I_{S,REF}$ ($= 3I_S$ here) so that

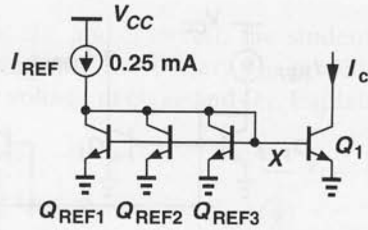

Figure 9.28 Copying a fraction of a reference current.

a unit transistor, Q_1, can generate a smaller current. Repeating the expressions in (9.89) and (9.90), we have

$$I_{REF} = 3I_S \exp \frac{V_X}{V_T} \tag{9.95}$$

$$I_{copy} = I_S \exp \frac{V_X}{V_T} \tag{9.96}$$

and hence

$$I_{copy} = \frac{1}{3} I_{REF}. \tag{9.97}$$

Example 9.15 It is desired to generate two currents equal to 50 μA and 500 μA from a reference of 200 μA. Design the current mirror circuit.

Solution To produce the smaller current, we must employ four unit transistors for Q_{REF} such that each carries 50 μA. A unit transistor thus generates 50 μA (Fig. 9.29). The current of 500 μA requires 10 unit transistors, denoted by $10A_E$ for simplicity.

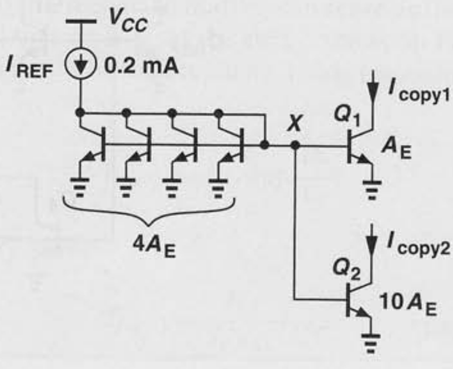

Figure 9.29

Exercise Repeat the above example for a reference current of 150 μA.

Effect of Base Current We have thus far neglected the base current drawn from node X in Fig. 9.26(a) by all transistors, an effect leading to a significant error as the

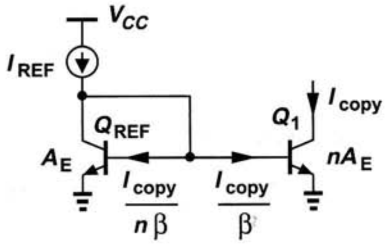

Figure 9.30 Error due to base currents.

number of copies (i.e., the total copied current) increases. The error arises because a fraction of I_{REF} flows through the bases rather than through the collector of Q_{REF}. We analyze the error with the aid of the diagram shown in Fig. 9.30, where A_E and nA_E denote one unit transistor and n unit transistors, respectively. Our objective is to calculate I_{copy}, recognizing that Q_{REF} and Q_1 still have equal base-emitter voltages and hence carry currents with a ratio of n. Thus, the base currents of Q_1 and Q_{REF} can be expressed as

$$I_{B1} = \frac{I_{copy}}{\beta} \tag{9.98}$$

$$I_{B,REF} = \frac{I_{copy}}{\beta} \cdot \frac{1}{n}. \tag{9.99}$$

Writing a KCL at X therefore yields

$$I_{REF} = I_{C,REF} + \frac{I_{copy}}{\beta} \cdot \frac{1}{n} + \frac{I_{copy}}{\beta}, \tag{9.100}$$

which, since $I_{C,REF} = I_{copy}/n$, leads to

$$I_{copy} = \frac{nI_{REF}}{1 + \frac{1}{\beta}(n+1)}. \tag{9.101}$$

For a large β and moderate n, the second term in the denominator is much less than unity and $I_{copy} \approx nI_{REF}$. However, as the copied current ($\propto n$) increases, so does the error in I_{copy}.

To suppress the above error, the bipolar current mirror can be modified as illustrated in Fig. 9.31. Here, emitter follower Q_F is interposed between the collector of Q_{REF} and node X, thereby reducing the effect of the base currents by a factor of β. More specifically, assuming $I_{C,F} \approx I_{E,F}$, we can repeat the above analysis by writing

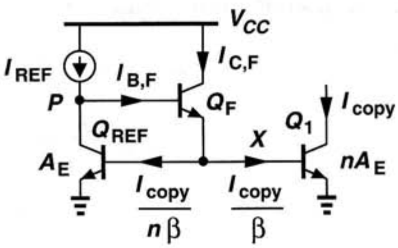

Figure 9.31 Addition of emitter follower to reduce error due to base currents.

a KCL at X:

$$I_{C,F} = \frac{I_{copy}}{\beta} + \frac{I_{copy}}{\beta} \cdot \frac{1}{n}, \tag{9.102}$$

obtaining the base current of Q_F as

$$I_{B,F} = \frac{I_{copy}}{\beta^2}\left(1 + \frac{1}{n}\right). \tag{9.103}$$

Another KCL at node P gives

$$I_{REF} = I_{B,F} + I_{C,REF} \tag{9.104}$$

$$= \frac{I_{copy}}{\beta^2}\left(1 + \frac{1}{n}\right) + \frac{I_{copy}}{n} \tag{9.105}$$

and hence

$$I_{copy} = \frac{nI_{REF}}{1 + \frac{1}{\beta^2}(n+1)}. \tag{9.106}$$

That is, the error is lowered by a factor of β.

Example 9.16

Compute the error in I_{copy1} and I_{copy2} in Fig. 9.29 before and after adding a follower.

Solution Noting that I_{copy1}, I_{copy2}, and $I_{C,REF}$ (the total current flowing through four unit transistors) still retain their nominal ratios (why?), we write a KCL at X:

$$I_{REF} = I_{C,REF} + \frac{I_{copy1}}{\beta} + \frac{I_{copy2}}{\beta} + \frac{I_{C,REF}}{\beta} \tag{9.107}$$

$$= 4I_{copy1} + \frac{I_{copy1}}{\beta} + \frac{10I_{copy1}}{\beta} + \frac{I_{C,REF}}{\beta}. \tag{9.108}$$

Thus,

$$I_{copy1} = \frac{I_{REF}}{4 + \frac{15}{\beta}} \tag{9.109}$$

$$I_{copy2} = \frac{10I_{REF}}{4 + \frac{15}{\beta}}. \tag{9.110}$$

With the addition of emitter follower (Fig. 9.32), we have at X:

$$I_{C,F} = \frac{I_{C,REF}}{\beta} + \frac{I_{copy1}}{\beta} + \frac{I_{copy2}}{\beta} \tag{9.111}$$

$$= \frac{4I_{copy1}}{\beta} + \frac{I_{copy1}}{\beta} + \frac{10I_{copy1}}{\beta} \tag{9.112}$$

$$= \frac{15I_{copy1}}{\beta}. \tag{9.113}$$

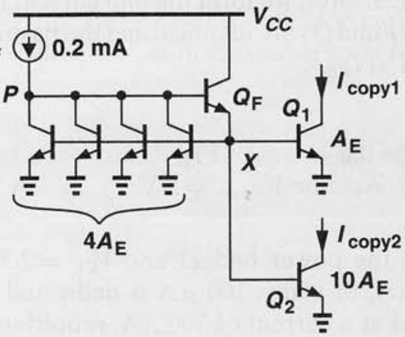

Figure 9.32

A KCL at P therefore yields

$$I_{REF} = \frac{15 I_{copy1}}{\beta^2} + I_{C,REF} \tag{9.114}$$

$$= \frac{15 I_{copy1}}{\beta^2} + 4 I_{copy1}, \tag{9.115}$$

and hence

$$I_{copy1} = \frac{I_{REF}}{4 + \frac{15}{\beta^2}} \tag{9.116}$$

$$I_{copy2} = \frac{10 I_{REF}}{4 + \frac{15}{\beta^2}}. \tag{9.117}$$

Exercise Calculate I_{copy1} if one of the four unit transistors is omitted, i.e., the reference transistor has an area of $3A_E$.

PNP Mirrors Consider the common-emitter stage shown in Fig. 9.33(a), where a current source serves as a load to achieve a high voltage gain. The current source can be realized as a *pnp* transistor operating in the active region [Fig. 9.33(b)]. We must therefore define the bias current of Q_2 properly. In analogy with the *npn* counterpart

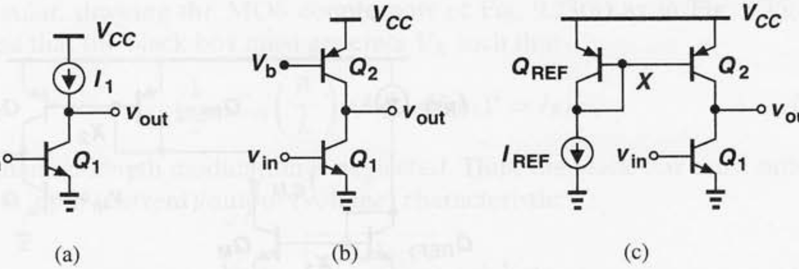

Figure 9.33 (a) CE stage with current-source load, (b) realization of current source by a *pnp* device, (c) proper biasing of Q_2.

of Fig. 9.23(c), we form the *pnp* current mirror depicted in Fig. 9.33(c). For example, if Q_{REF} and Q_2 are identical and the base currents negligible, then Q_2 carries a current equal to I_{REF}.

Example 9.17

Design the circuit of Fig. 9.33(c) for a voltage gain of 100 and a power budget of 2 mW. Assume $V_{A,npn} = 5$ V, $V_{A,pnp} = 4$ V, $I_{REF} = 100\ \mu$A, and $V_{CC} = 2.5$ V.

Solution

From the power budget and $V_{CC} = 2.5$ V, we obtain a total supply current of 800 μA, of which 100 μA is dedicated to I_{REF} and Q_{REF}. Thus, Q_1 and Q_2 are biased at a current of 700 μA, requiring that the (emitter) area of Q_2 be 7 times that of Q_{REF}. (For example, Q_{REF} incorporates one unit device and Q_1 seven unit devices.)

The voltage gain can be written as

$$A_v = -g_{m1}(r_{O1}||r_{O2}) \tag{9.118}$$

$$= -\frac{1}{V_T} \cdot \frac{V_{A,npn}V_{A,pnp}}{V_{A,npn} + V_{A,pnp}} \tag{9.119}$$

$$= -85.5. \tag{9.120}$$

What happened here?! We sought a gain of 100 but inevitably obtained a value of 85.5! This is because the gain of the stage is simply given by the Early voltages and V_T, a fundamental constant of the technology and independent of the bias current. Thus, with the above choice of Early voltages, the circuit's gain cannot reach 100.

Exercise What Early voltage is necessary for a voltage gain of 100?

We must now address an interesting problem. In the mirror of Fig. 9.23(c), it is assumed that the golden current flows from V_{CC} to node X, whereas in Fig. 9.33(c) it flows from X to ground. How do we generate the latter from the former? It is possible to combine the *npn* and *pnp* mirrors for this purpose, as illustrated in Fig. 9.34. Assuming for simplicity that Q_{REF1}, Q_M, Q_{REF2}, and Q_2 are identical and neglecting the base currents, we observe that Q_M draws a current of I_{REF} from Q_{REF2}, thereby forcing the same current through Q_2 and Q_1. We can also create various scaling scenarios between Q_{REF1} and Q_M and between Q_{REF2} and Q_2. Note that the base currents introduce a cumulative error as I_{REF} is copied onto $I_{C,M}$, and $I_{C,M}$ onto I_{C2}.

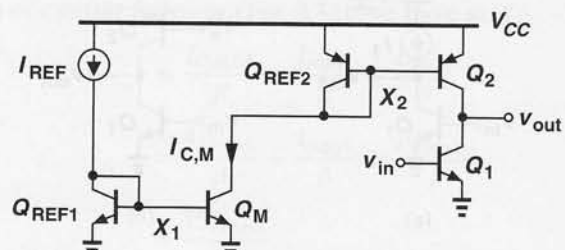

Figure 9.34 Generation of current for *pnp* devices.

Example 9.18

We wish to bias Q_1 and Q_2 in Fig. 9.34 at a collector current of 1 mA while $I_{REF} = 25\ \mu A$. Choose the scaling factors in the circuit so as to minimize the number of unit transistors.

Solution For an overall scaling factor of $1\ mA/25\ \mu A = 40$, we can choose either

$$I_{C,M} = 8I_{REF} \tag{9.121}$$

$$|I_{C2}| = 5I_{C,M} \tag{9.122}$$

or

$$I_{C,M} = 10I_{REF} \tag{9.123}$$

$$|I_{C2}| = 4I_{C,M}. \tag{9.124}$$

(In each case, the *npn* and *pnp* scaling factors can be swapped.) In the former case, the four transistors in the current mirror circuitry require 15 units, and in the latter case, 16 units. Note that we have implicitly dismissed the case $I_{C,M} = 40I_{C,REF1}$ and $I_{C2} = I_{C,REF2}$ as it would necessitate 43 units.

Exercise Calculate the exact value of I_{C2} if $\beta = 50$ for all transistors.

Example 9.19

An electrical engineering student purchases two nominally identical discrete bipolar transistors and constructs the current mirror shown in Fig. 9.23(c). Unfortunately, I_{copy} is 30% higher than I_{REF}. Explain why.

Solution It is possible that the two transistors were fabricated in different batches and hence underwent slightly different processing. Random variations during manufacturing may lead to changes in the device parameters and even the emitter area. As a result, the two transistors suffer from significant I_S mismatch. This is why current mirrors are rarely used in discrete design.

Exercise How much I_S mismatch results in a 30% collector current mismatch?

9.2.3 MOS Current Mirror

The developments in Section 9.2.2 can be applied to MOS current mirrors as well. In particular, drawing the MOS counterpart of Fig. 9.23(a) as in Fig. 9.35(a), we recognize that the black box must generate V_X such that

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_X - V_{TH1})^2 = I_{REF}, \tag{9.125}$$

where channel-length modulation is neglected. Thus, the black box must satisfy the following input (current)/output (voltage) characteristic:

$$V_X = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{TH1}. \tag{9.126}$$

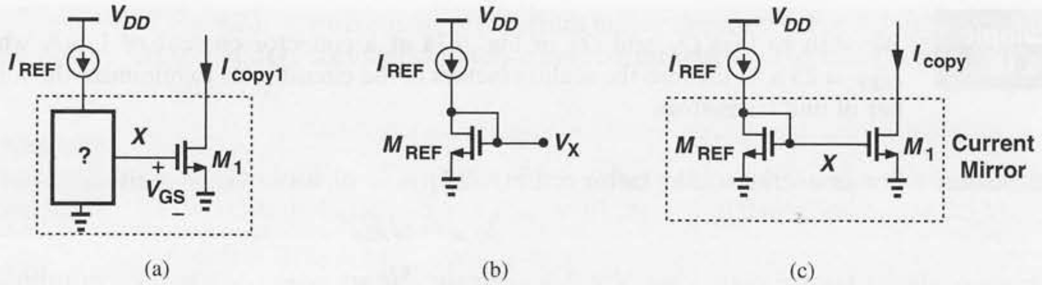

Figure 9.35 (a) Conceptual illustration of copying a current by an NMOS device, (b) generation of a voltage proportional to square root of current, (c) MOS current mirror.

That is, it must operate as a "square-root" circuit. From Chapter 6, we recall that a diode-connected MOSFET provides such a characteristic [Fig. 9.35(b)], thus arriving at the NMOS current mirror depicted in Fig. 9.35(c). As with the bipolar version, we can view the circuit's operation from two perspectives: (1) M_{REF} takes the square root of I_{REF} and M_1 squares the result; or (2) the drain currents of the two transistors can be expressed as

$$I_{D,REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{REF}(V_X - V_{TH})^2 \tag{9.127}$$

$$I_{copy} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_X - V_{TH})^2, \tag{9.128}$$

where the threshold voltages are assumed equal. It follows that

$$I_{copy} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{REF}} I_{REF}, \tag{9.129}$$

which reduces to $I_{copy} = I_{REF}$ if the two transistors are identical.

Example 9.20

The student working on the circuits in Examples 9.12 and 9.13 decides to try the MOS counterpart, thinking that the gate current is zero and hence leaving the gates floating (Fig. 9.36). Explain what happens.

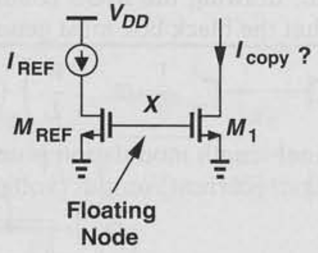

Figure 9.36

Solution This circuit is not a current mirror because only a diode-connected device can establish (9.129) and hence a copy current independent of device parameters and temperature. Since the gates of M_{REF} and M_1 are floating, they can assume any voltage, e.g., an initial condition created at node X when the power supply is turned on. In other words, I_{copy} is very poorly defined.

Exercise Is M_{REF} always off in this circuit?

Generation of additional copies of I_{REF} with different scaling factors also follows the principles shown in Fig. 9.26. The following example illustrates these concepts.

Example 9.21 An integrated circuit employs the source follower and the common-source stage shown in Fig. 9.37(a). Design a current mirror that produces I_1 and I_2 from a 0.3-mA reference.

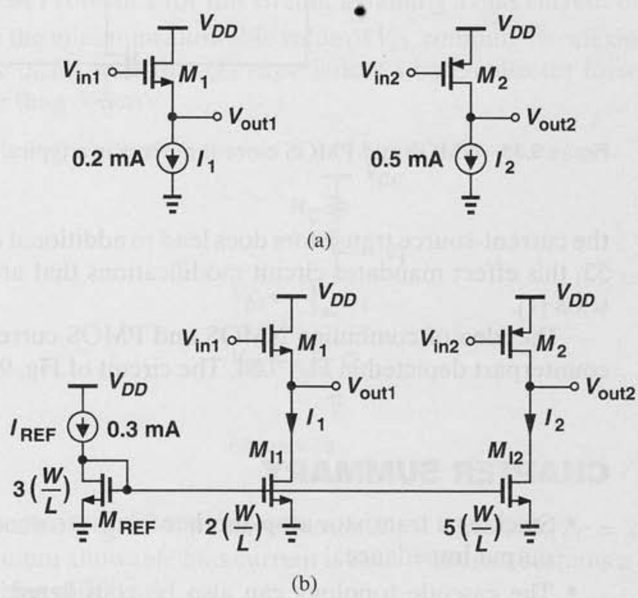

Figure 9.37

Solution Following the methods depicted in Figs. 9.28 and 9.29, we select an aspect ratio of $3(W/L)$ for the diode-connected device, $2(W/L)$ for M_{I1}, and $5(W/L)$ for M_{I2}. Figure 9.37(b) shows the overall circuit.

Exercise Repeat the above example if $I_{REF} = 0.8$ mA.

Since MOS devices draw a negligible gate current,[6] MOS mirrors need not resort to the technique shown in Fig. 9.31. On the other hand, channel-length modulation in

[6]In deep-submicron CMOS technologies, the gate oxide thickness is reduced to less than 30 Å, leading to "tunneling" and hence noticeable gate current. This effect is beyond the scope of this book.

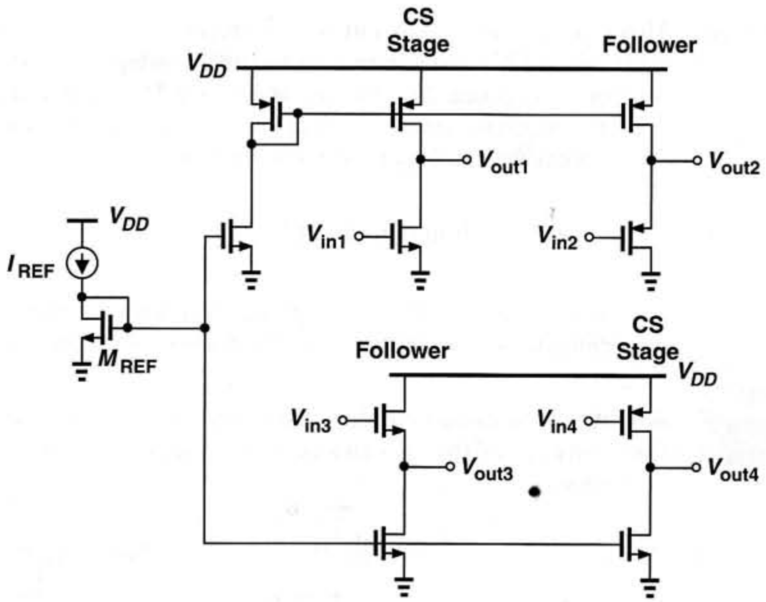

Figure 9.38 NMOS and PMOS current mirrors in a typical circuit.

the current-source transistors does lead to additional errors. Investigated in Problem 53, this effect mandates circuit modifications that are described in more advanced texts [1].

The idea of combining NMOS and PMOS current mirrors follows the bipolar counterpart depicted in Fig. 9.34. The circuit of Fig. 9.38 exemplifies these ideas.

9.3 CHAPTER SUMMARY

- Stacking a transistor atop another forms a cascode structure, resulting in a high output impedance.
- The cascode topology can also be considered an extreme case of source or emitter degeneration.
- The voltage gain of an amplifier can be expressed as $-G_m R_{out}$, where G_m denotes the short-circuit transconductance of the amplifier. This relationship indicates that the gain of amplifiers can be maximized by maximing their output impedance.
- With its high output impedance, a cascode stage can operate as a high-gain amplifier.
- The load of a cascode stage is also realized as a cascode circuit so as to approach an ideal current source.
- Setting the bias currents of analog circuits to well-defined values is difficult. For example, resistive dividers tied to the base or gate of transistors result in supply- and temperature-dependent currents.
- If V_{BE} or V_{GS} are well-defined, then I_C or I_D are not.
- Current mirrors can "copy" a well-defined reference current numerous times for various blocks in an analog system.

9.2 CURRENT MIRRORS

9.2.1 Initial Thoughts

The biasing techniques studied for bipolar and MOS amplifiers in Chapters 4 and 6 prove inadequate for high-performance microelectronic circuits. For example, the bias current of CE and CS stages is a function of the supply voltage—a serious issue because in practice, this voltage experiences some variation. The rechargeable battery in a cellphone or laptop computer, for example, gradually loses voltage as it is discharged, thereby mandating that the circuits operate properly across a *range* of supply voltages.

Another critical issue in biasing relates to ambient temperature variations. A cellphone must maintain its performance at −20°C in Finland and +50°C in Saudi Arabia. To understand how temperature affects the biasing, consider the bipolar current source shown in Fig. 9.21(a), where R_1 and R_2 divide V_{CC} down to the required V_{BE}. That is, for a desired current I_1, we have

$$\frac{R_2}{R_1 + R_2} V_{CC} = V_T \ln \frac{I_1}{I_S}, \tag{9.83}$$

where the base current is neglected. But, what happens if the temperature varies? The left-hand side remains constant if the resistors are made of the same material and hence vary by the same percentage. The right-hand side, however, contains two temperature-dependent parameters: $V_T = kT/q$ and I_S. Thus, even if the base-emitter voltage remains constant with temperature, I_1 does not.

A similar situation arises in CMOS circuits. Illustrated in Fig. 9.21(b), a MOS current source biased by means of a resistive divider suffers from dependence on V_{DD} and temperature. Here, we can write

$$I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{9.84}$$

$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1 + R_2}V_{DD} - V_{TH}\right)^2. \tag{9.85}$$

Since both the mobility and the threshold voltage vary with temperature, I_1 is not constant even if V_{GS} is.

In summary, the typical biasing schemes introduced in Chapters 4 and 6 fail to establish a constant collector or drain current if the supply voltage or the ambient temperature are subject to change. Fortunately, an elegant method of creating supply- and temperature-independent voltages and currents exists and appears in almost all microelectronic systems. Called the "bandgap reference circuit" and employing several tens of devices, this scheme is studied in more advanced books [1].

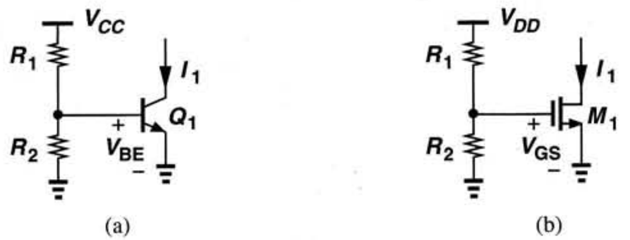

Figure 9.21 Impractical biasing of (a) bipolar and (b) MOS current sources.